

FIG. 3

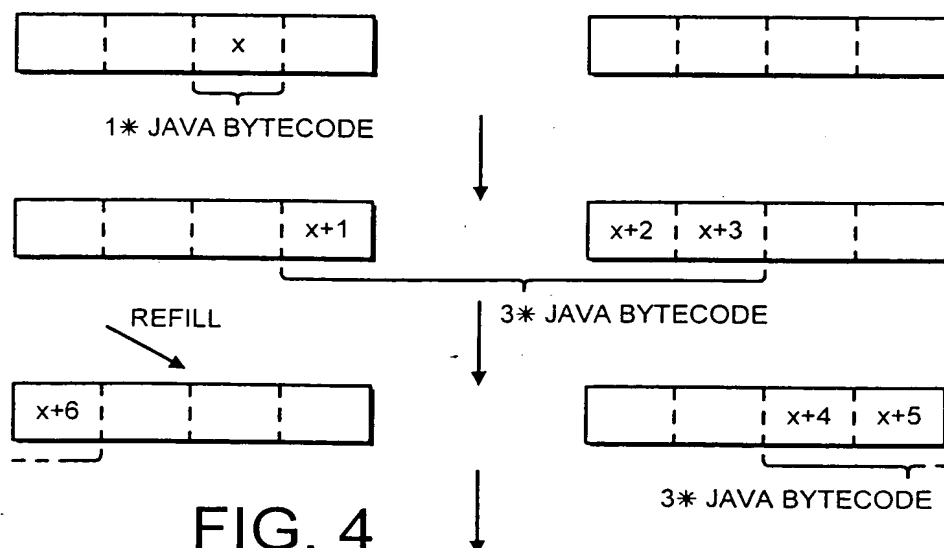


FIG. 4

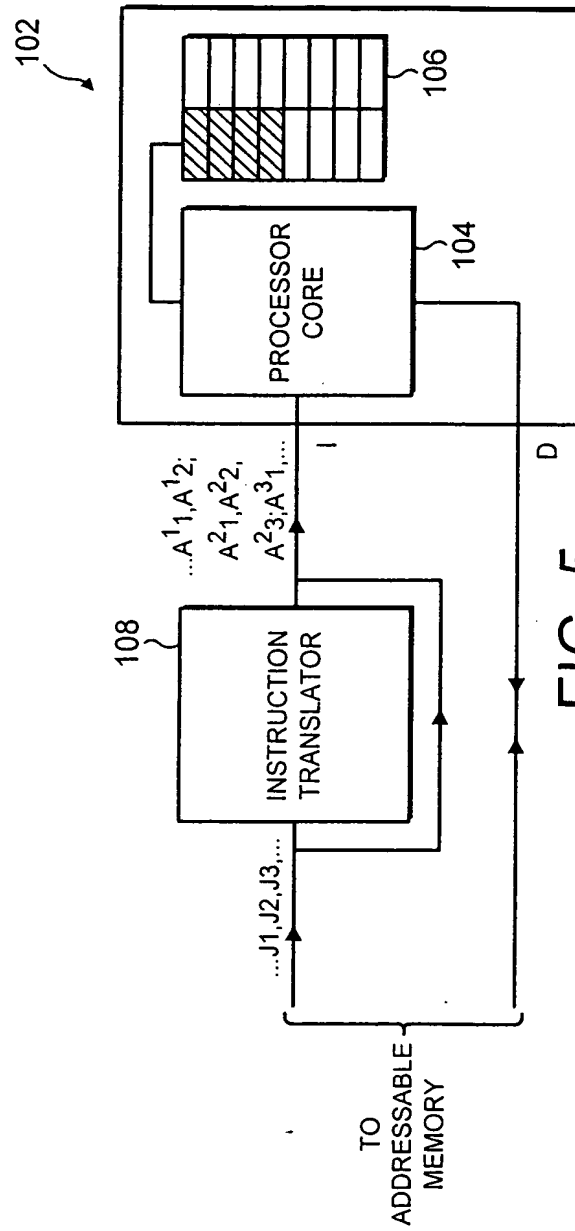


FIG. 5

JAVA INSTRUCTION	iadd (RF=2, RF>0)	iadd (RF=2, RF>1)	iadd (SA=-1)
ARM INSTRUCTION(S)	LDR R0[RStack, #4]! (POP)	LDR R3[RStack, #4]! (POP)	ADD R3, R3, R0
STATE	00000	00100	01000
R0	E	SOA TOS	SOA TOS
R1	E	E	E
R2	E	E	E
R3	E	E	(SOA+SOB) TOS

	lload <sup>1</sup> (RF=0, RE>2)	lload <sup>2</sup> (RF=0, RE>2)	lload <sup>2</sup> (RF=0, RE=2)
JAVA INSTRUCTION	LDR R1[Rvars, #4] LDR R0[Rvars, #0]	STR R3[RStack, #4] (PUSH)	LDR R3[Rvars, #4] LDR R2[Rvars, #0]
STATE	00000	00100	01000
R0	E	SOA TOS-1	SOA TOS-1
R1	E	SOA TOS	SOA TOS
R2	E	E	E
R3	(SOA+SOB) TOS	(SOA+SOB) TOS	SOA TOS

FIG. 6

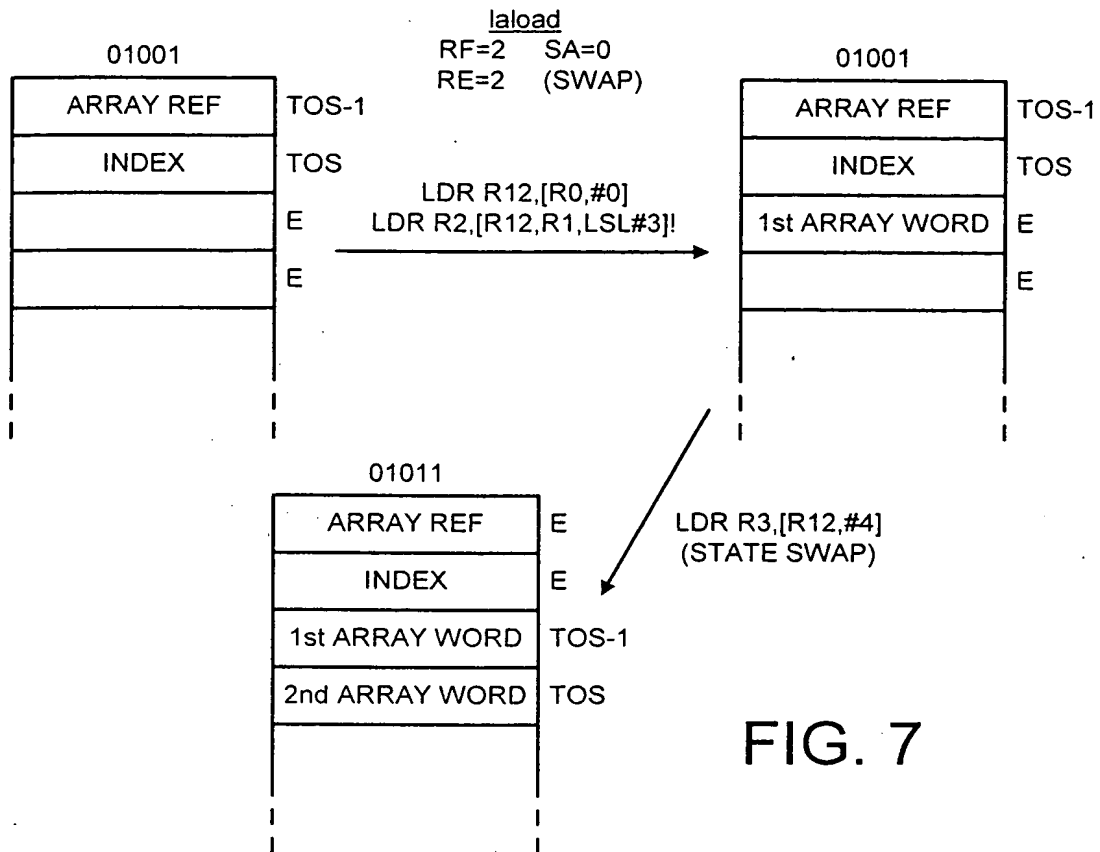


FIG. 7

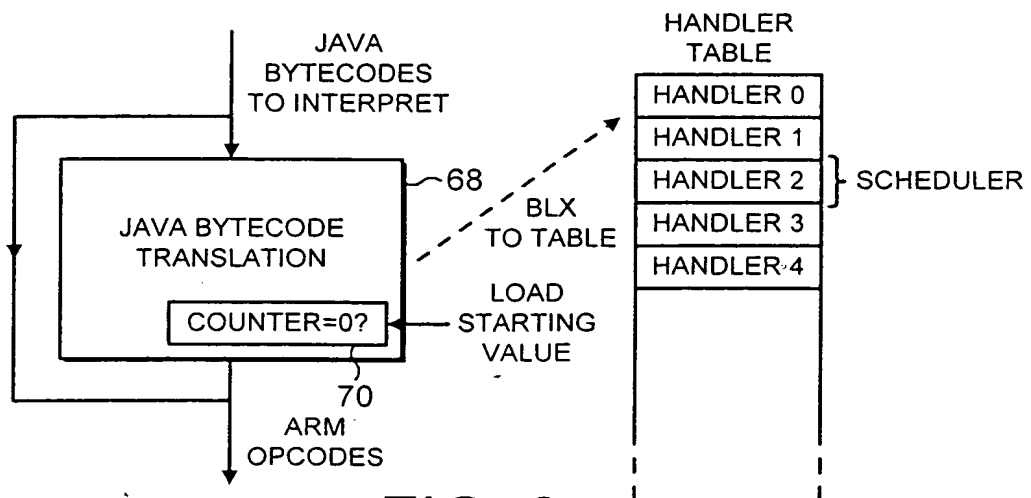


FIG. 9

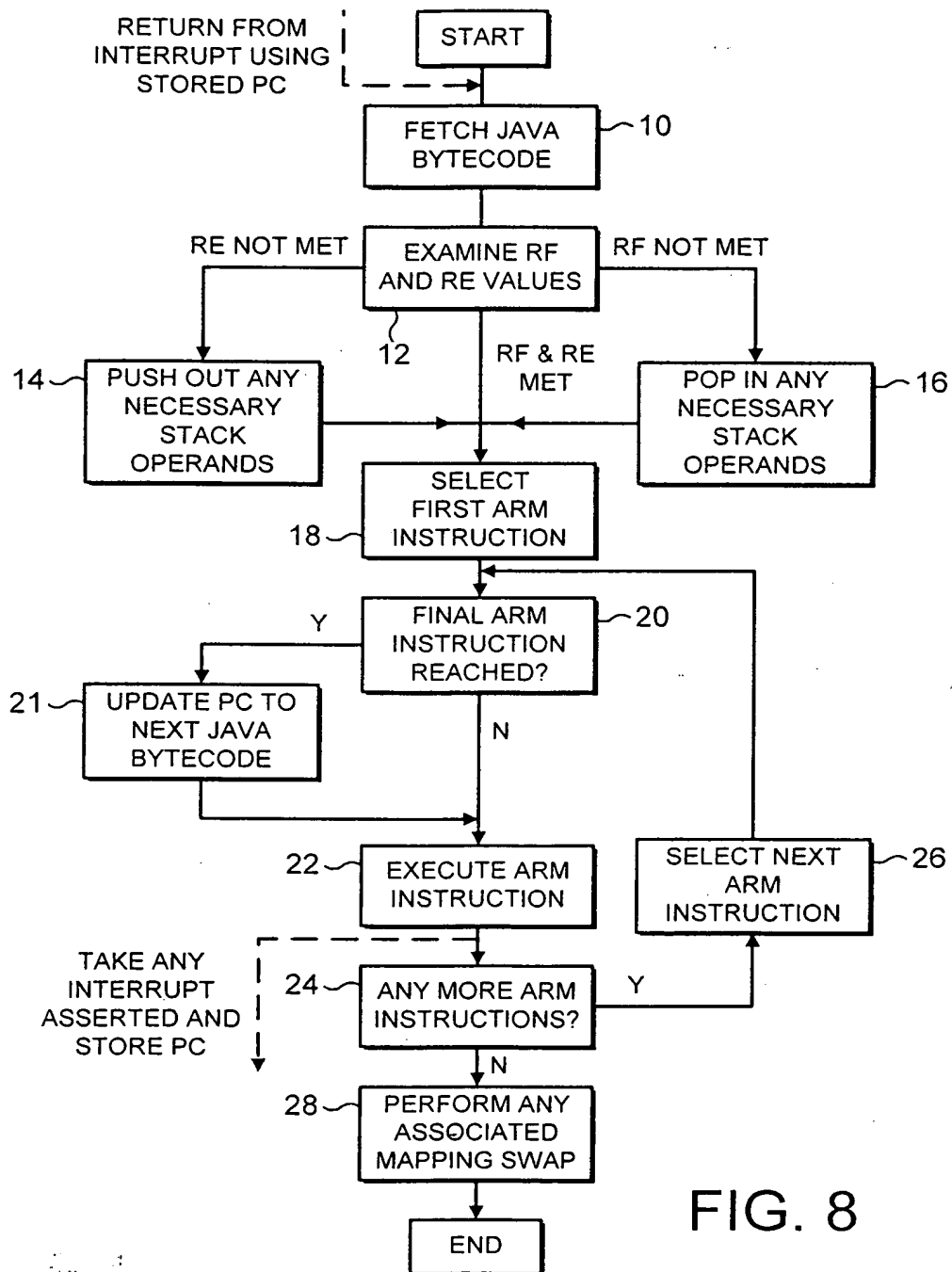


FIG. 8

094950 0907E260

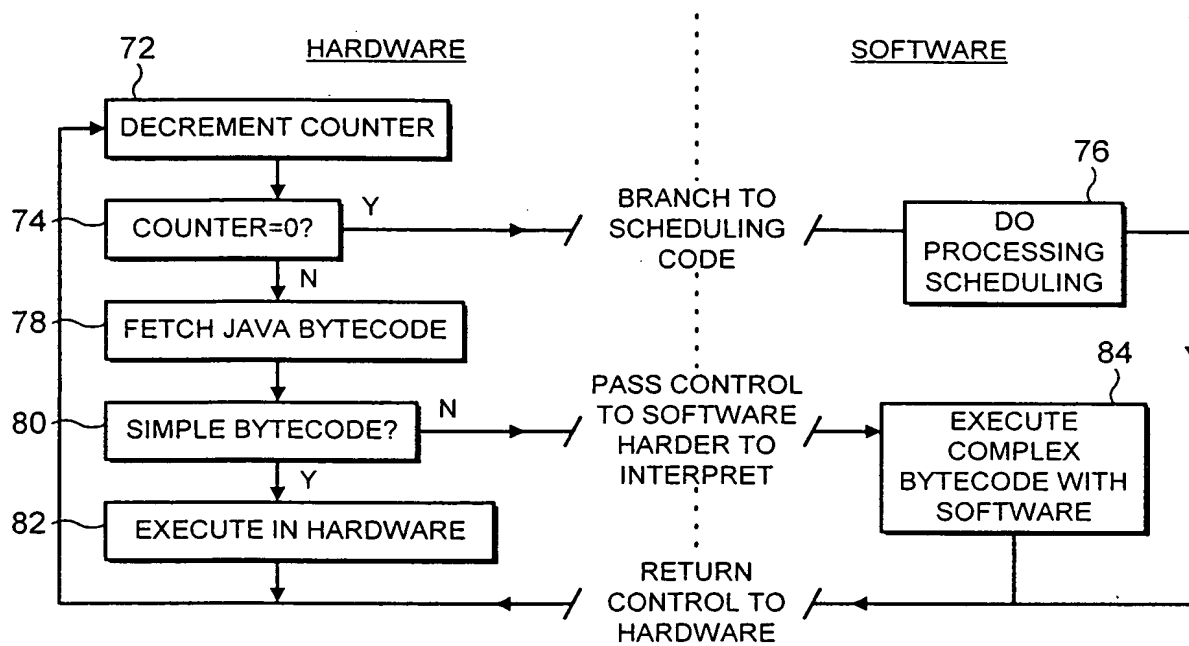


FIG. 10

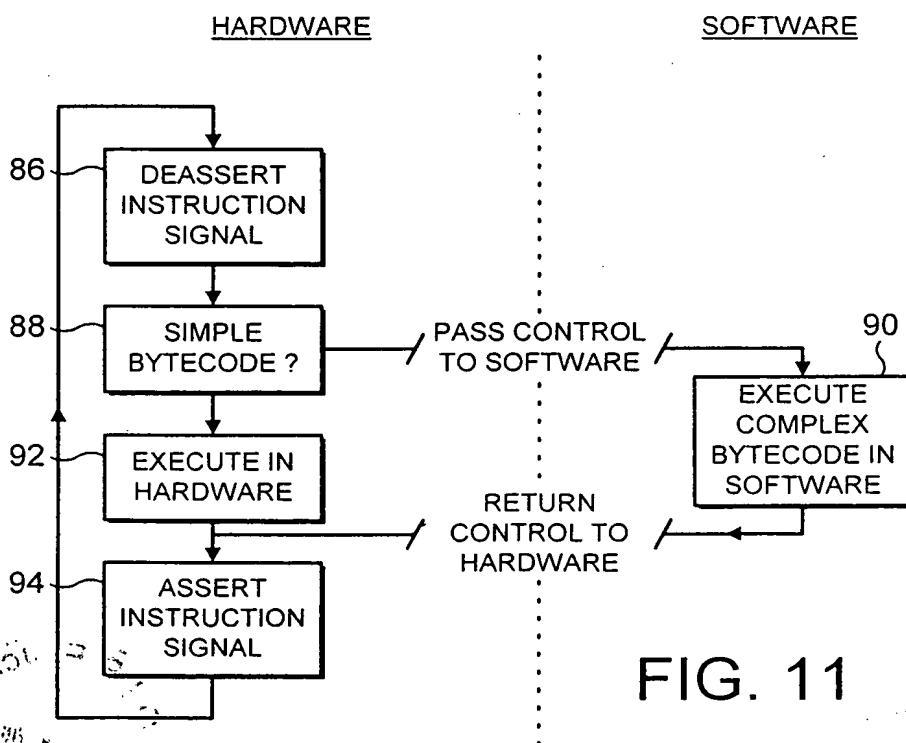


FIG. 11

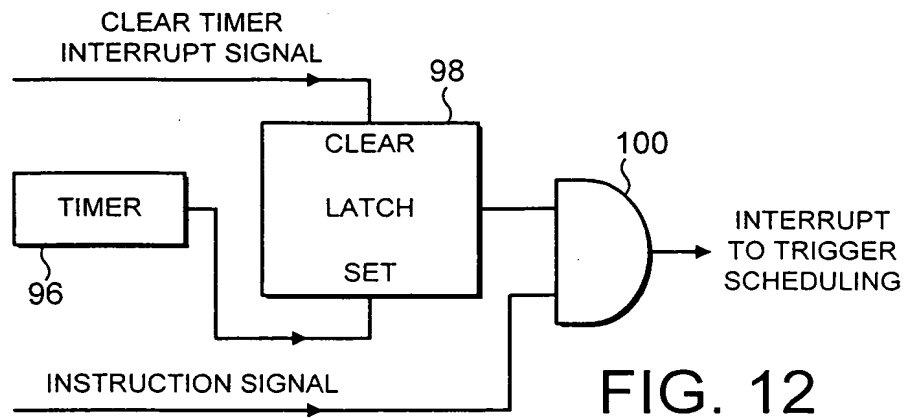


FIG. 12

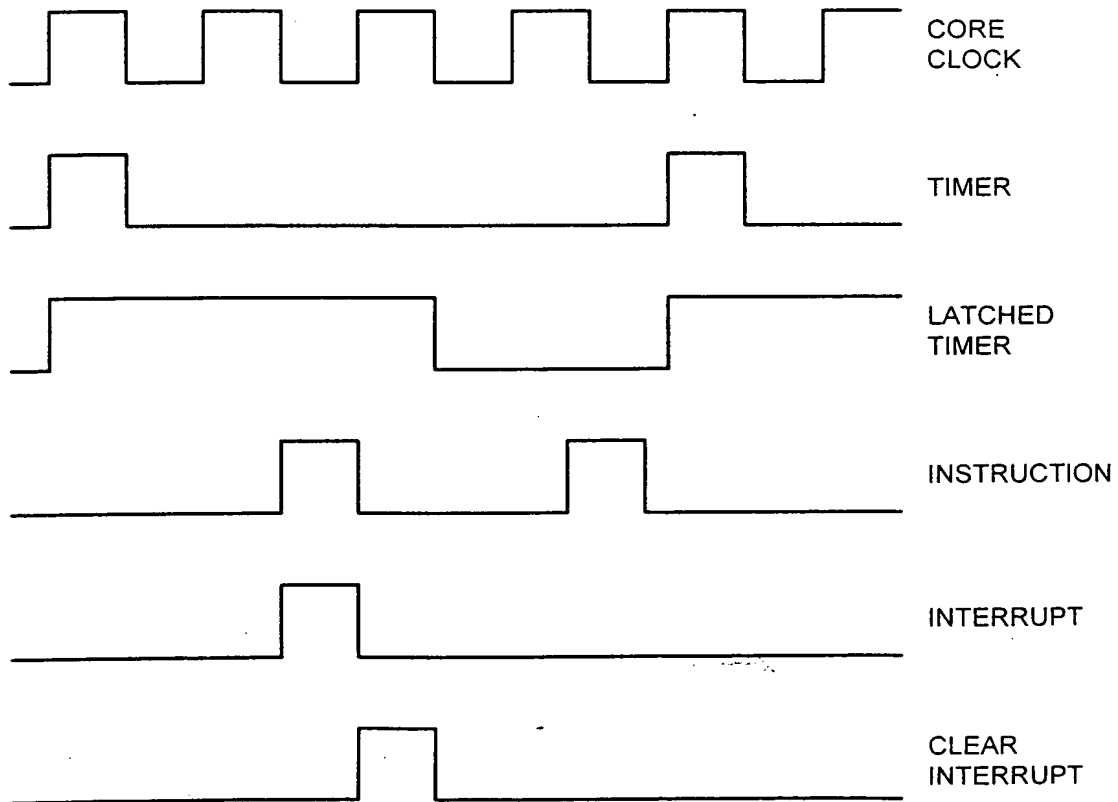


FIG. 13

0974050 022901